BASIC OF SIGNAL INTEGRITY
PART I - EYE DIAGRAM AND JITTER ANALYSIS

“There are 2 kinds of designers, those with signal integrity problems and those that will have them” *

April 2020
Tommaso Tessitore

* from a whiteboard at a major company

AGENDA

- ► Serial Standard Overview
- ► Signal Integrity test
  - – Design Constrains
  - – Common Blocks
- ► Eye diagram
  - – What is an Eye Diagram
  - – Metodology for Eye Diagram Measurements
- ► Motivation for Jitter Decomposition
  - – What is Jitter
  - – Jitter components
  - – How measure Jitter
- ► Methodology for Jitter Measurements
- ► R&S Jitter decomposition/measurement approach
- ► Live demo – Eye diagram and jitter measurements on a High Speed device
- ► Summary and Q&A

SERIAL STANDARD OVERVIEW

HIGH SPEED DATA LINK DEMANDS

- Fast serial buses have replaced many parallel buses
  - Fast serial signals were found mostly in Telecom and Datacom industries. They now span several industries including Computer, Consumer, Aerospace & Defence and even more Automotive.
  - Serial Transmission applications range from hundreds of MHz to tens/hundreds of GHz.

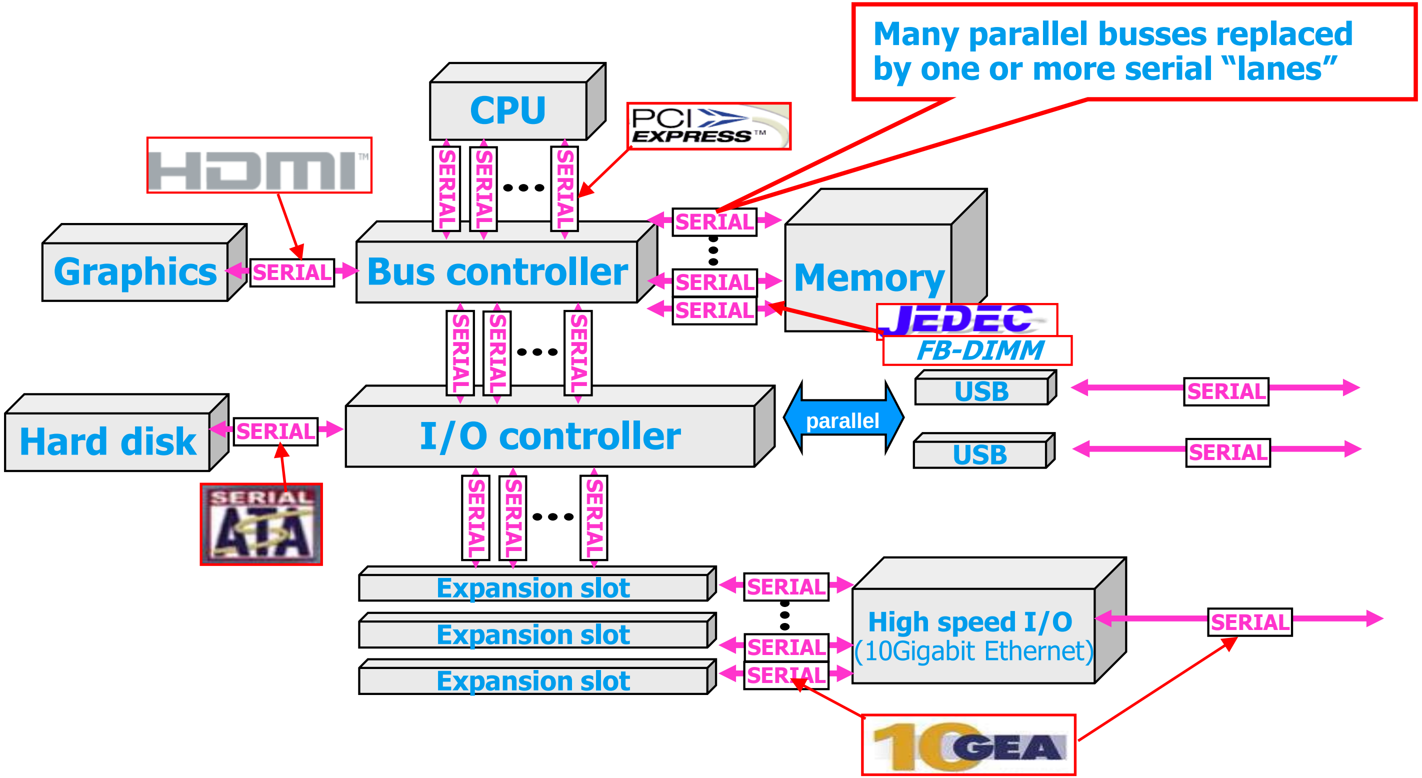
A WORLD OF STANDARDS……

Standard	Electrical Serial Line Rate	Link	Lanes
PCIe 3.0	8 Gbps	Chip-to-chip and backplane	1, 2, 4, 8
PCIe 2.0	5 Gbps	Ch	
Interlaken	4.976 Gbps to 6.375 Gbps	Ch	
Serial RapidIO® 2.0+	1.25, 2.5, 3.125, 5 to 6.25 Gbps	Ch	
CPRI 4.0+	0.6144, 1.2288, 2.4576, 3.072, 4.9152, 6.144 Gbps		
OBSAI 4.0+ (RP3)	0.768, 1.536, 3.072, 6.144 Gbps	Ch	
SATA 3.0	6 Gbps	Ch	
SAS 2.0	6 Gbps	Ch	
SPAUI	6.375 Gbps	Ch	
DDR-XAUI	6.25 Gbps	Ch	
QPI	4, 4.8, 6.4, 8 Gbps		
HyperTransport 3.0+	0.4, 2.4, 2.8, 3.2 Gbps	Ch	
HighGig+, HighGig2+	3.75, 6.25 Gbps	Ch	
8G FC	8.5 Gbps	Chip	
OIF/CEI 6			
OIF/CEI 6			
4G FC			

Standard	Electrical Serial Line Rate	Link	Lanes
IEEE 802.3ba 40G	10.3125 Gbps	Chip-to-chip, backplane	4
IEEE 802.3ba 100G	10.3125 Gbps	Chip-to-module	10
IEEE 802.3ba 10GBASE-R	10.3125 Gbps	Chip-to-module	1 to N
IEEE 802.3ba 10GBASE-KR	10.3125 Gbps	Backplane	1 to N
10G GPON/EPON	10 Gbps	Chip-to-chip, chip-to-module	1 to N
OIF SFI-S	9.95 to 11.1 Gbps	Chip-to-module	(8, 10, 12, 16)+1
OIF SFI-5.2 (40G)	9.95 to 11.1 Gbps	Chip-to-module	5
10G Interlaken	10.6921 Gbps	Chip-to-chip, cable	1 to N
SONET/SDH OC-192 (10G)	9.95 Gbps	Chip-to-chip	1 to N
SONET/SDH OC-192 (40G)	9.95 Gbps	Chip-to-chip	4
SFP+	8.5 to 11.32 Gbps	Optical module std	1 to N
XFP	9.95328 to 1 1/32 Gbps	Optical module std	1 to N
OIF/CEI 11G-SR	9.95 to 11.1 Gbps	Chip-to-chip	I/O technology
OIF/CEI 11G-LR	9.95 to 11.1 Gbps	Backplane	I/O technology
OTU2	10.709 Gbps	Chip-to-chip	See SFI-S
OTU3	10.7545 Gbps	SFI-S	See SFI-S
			FI-S
			N
			N

Standard	Electrical Serial Line Rate	Link	Lanes
OIF/CEI 28G-SR	19.9-28 Gbps	Chip-to-chip	1 to N
OIF/CEI 28G-VSR	19.9-28 Gbps	chip-to-module	1 to N
IEEE 802.3ba 100G	25 Gbps	Chip-to-chip, chip-to-module, cable	4
32G FibreChannel	28 Gbps	chip-to-module	1 to N
25G InfiniBand	25 Gbps	Chip-to-chip, chip-to-module, cable	1 to N

APPLICATION EXAMPLE



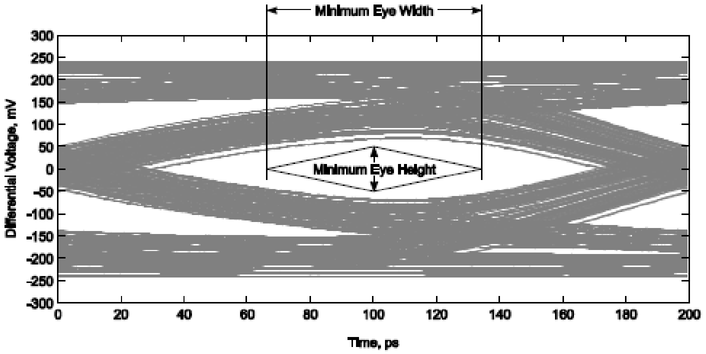
SIGNAL INTEGRITY TEST

SIGNAL INTEGRITY TEST

- ► Eye Diagram Mask Test and Jitter Separation are common measurements for many standards, e.g.:
  - – USB3.2
  - – PCIe
  - – HDMI, etc.

- ► Developer require Mask Tes and Jitter Separation for compliance and for debugging:
  - – Does the design meet the specs?
  - – What is the root cause of the transmission / signal integrity issue

Figure 6-17. Eye Masks



Gen 1 eye mask

USB specification define Eye Diagram Mask Test

Table 4-4: Total System Jitter Budget for 5.0 GT/s Signaling

Jitter Contribution	Max RMS Rj (ps)	Max Dj (ps)	Tj at BER 10^{-12} (ps)
Tx	1.4	30	50
Ref Clock	3.1	0	43.6
Media	0	58	58
Rx	1.4	60	80
Linear Total Tj:			231.6
Root Sum Square (RSS) Total Tj:			200

USB specification require RJ, DJ and TJ @ 10^{-12}

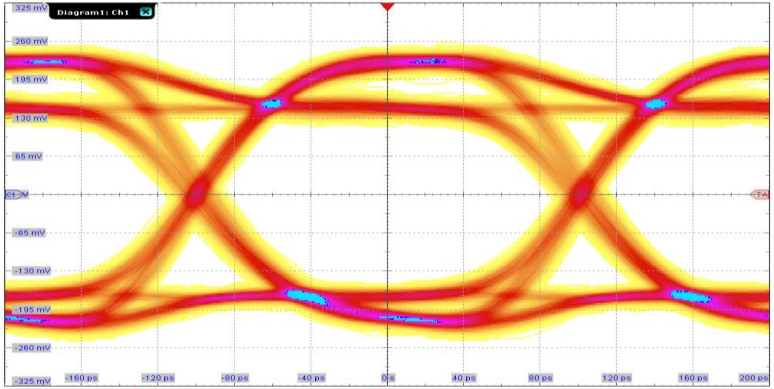
GET IT RIGHT THE FIRST TIME !

- **Always the goal !!!**
- What does “Get it Right” mean?
  - Avoid going “back to the drawing board”
  - Avoid costly and time-consuming re-spins
  - Manage the risk
  - … last but not least, avoid making your boss look bad
- Models, simulation, etc. helps, but…..

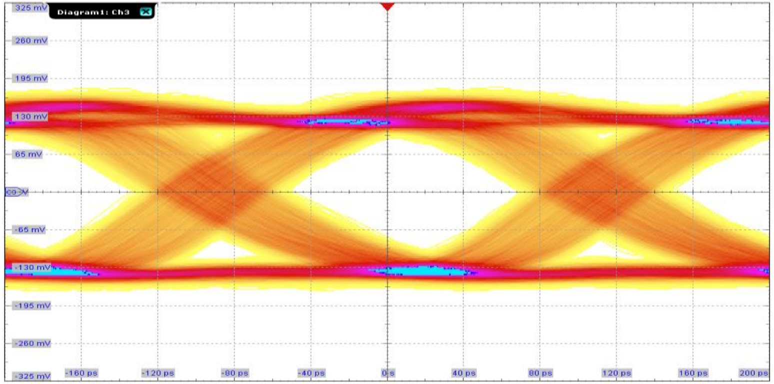
- …. sometimes the unimaginable failure occurs – and we need to deal with it.
- It is the case for cutting edge, state-of-the-art designs..

UNFORTUNATELY, THE TEST SHOWS A FAILURE

► Expect signal to look like this:



► But you see this :



OK WE HAVE A FAILURE. WHAT NOW?

- Step 1: (attempt to) Soothe the fears of your manager(s)

- Step 2: Implement your **debug plan.**

Debugging Can't be avoided !!

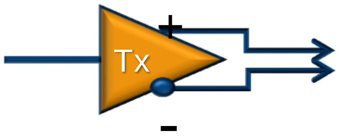
- Obviously you cannot plan for all circumstances, but:
  - Ensure you have the right equipments
  - Understand the debug capabilities of your instruments
  - **Design for debug**: test points, interposers, fixture, S-parameter model, etc.

SERIAL DATA COMMON BLOCKS

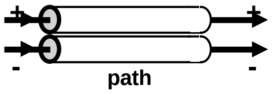
- Let's define a simple set of building blocks for the serial data physical layer.
- It helps to establish a common language for quickly describing the most frequently encountered test scenarios and challenges.

Transmitters

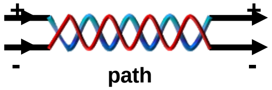
Differential
Transmitter



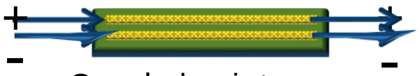
Interconnects (paths - Channel)



Dual-coax
differential cable



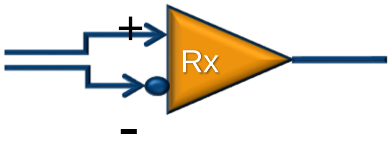
Twisted-pair
differential cable



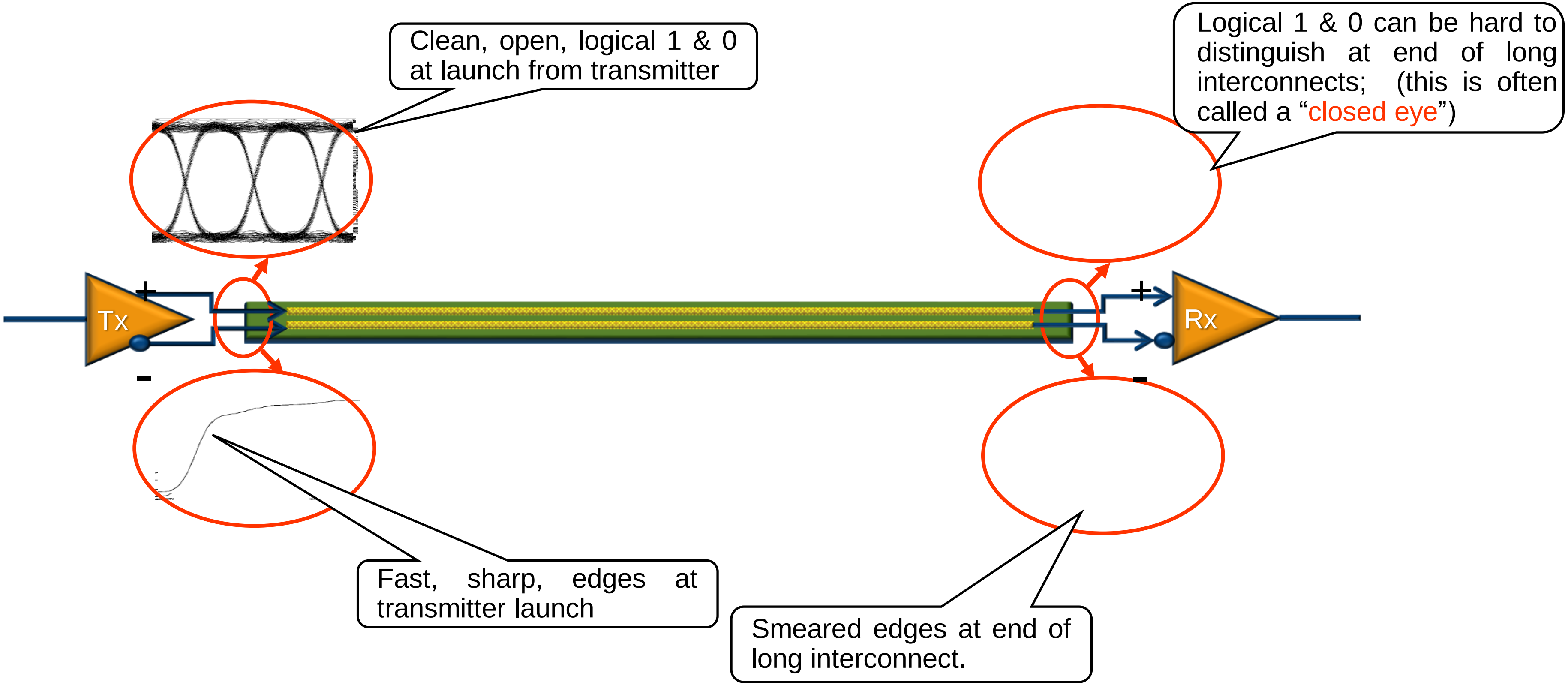
Coupled-pair traces on **circuit board** (backplanes)

Receivers

Differential
Receiver

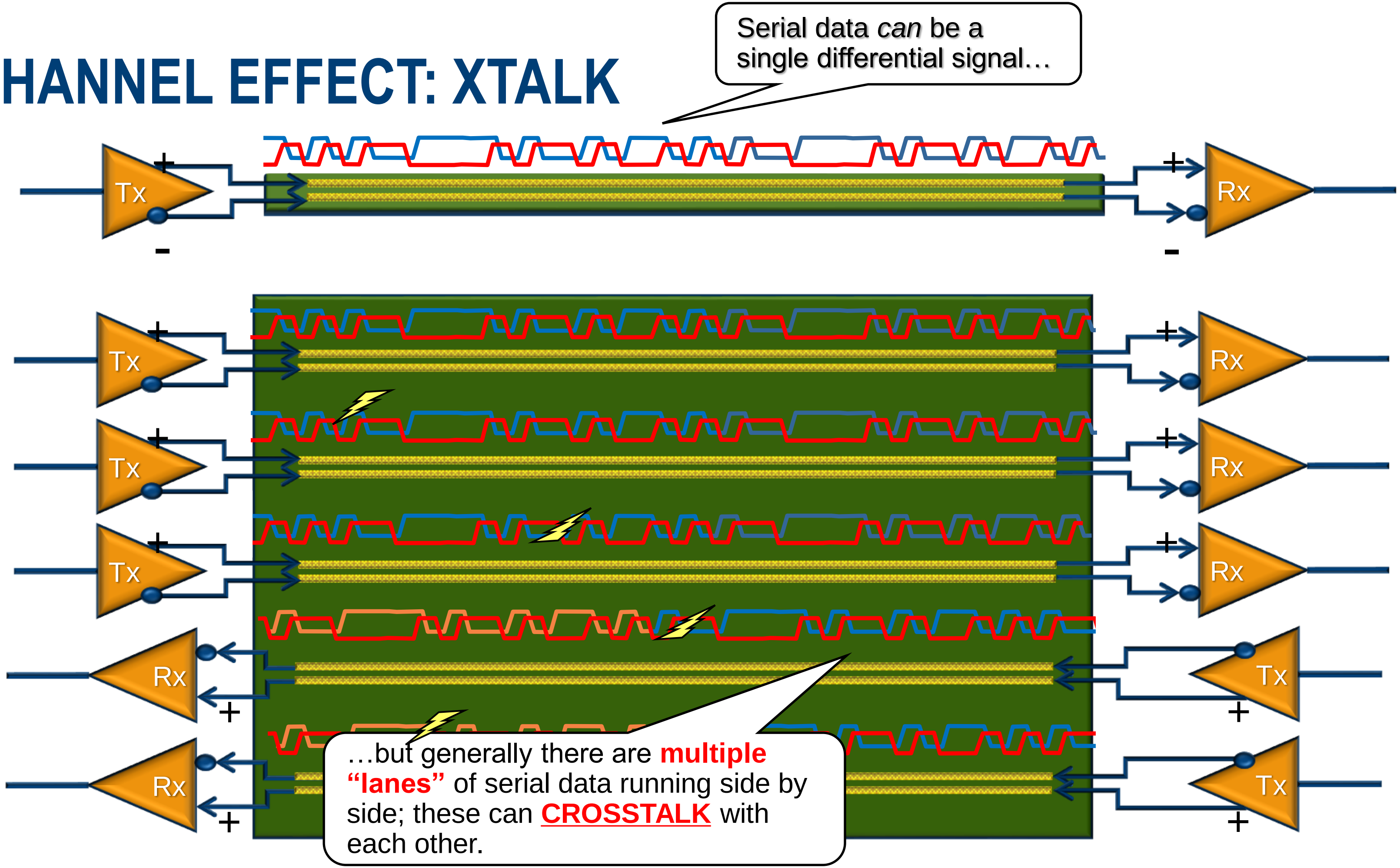


CHANNEL EFFECT: LOSS AND DISPERSION



The faster the data rate and the longer the interconnect, then the more loss in the signal

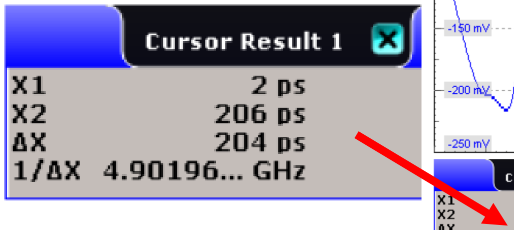
CHANNEL EFFECT: XTALK

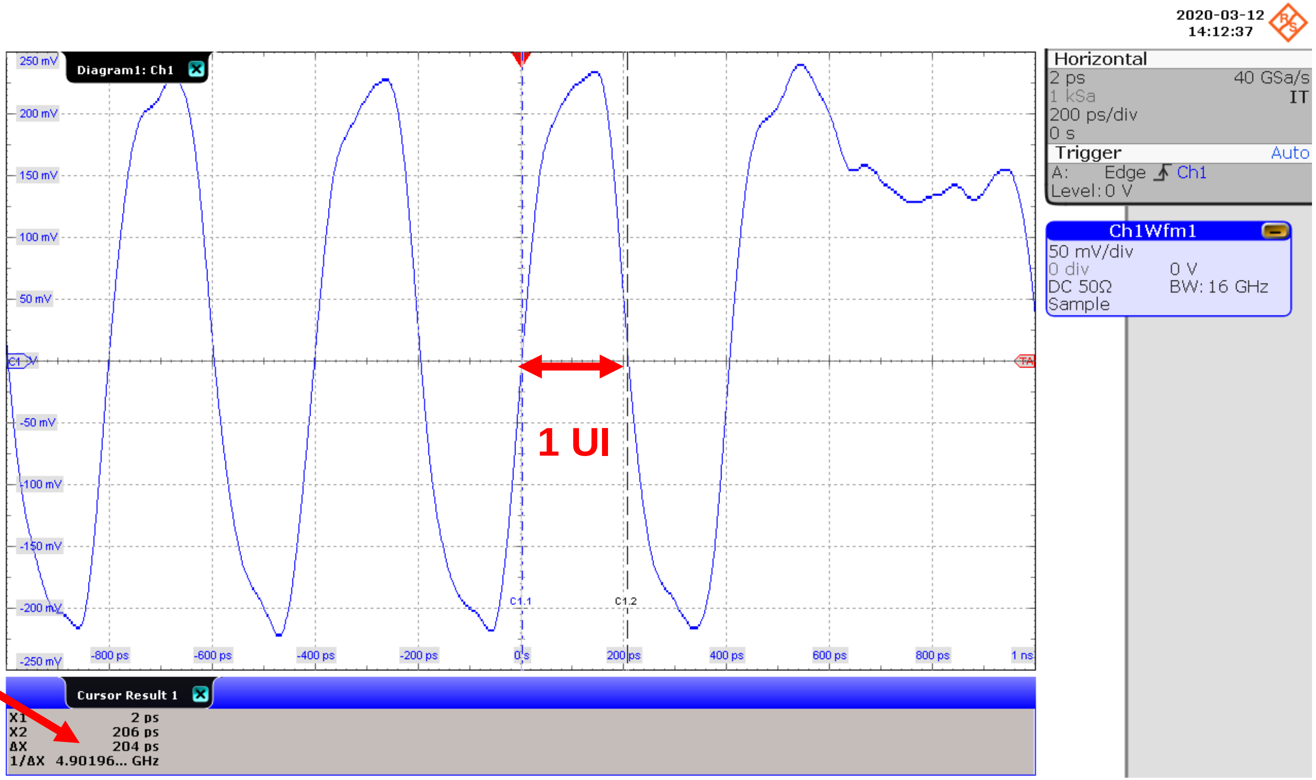


EYE DIAGRAM

WHAT IS A UNIT INTERVAL

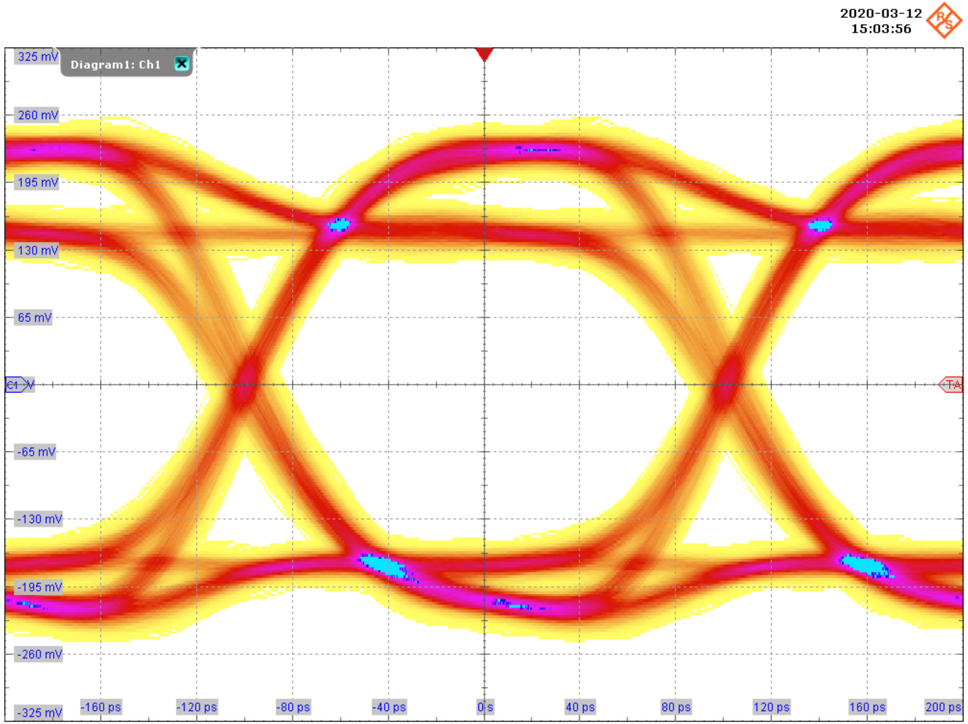
- A Unit Interval (UI) is the period of 1 bit of a data signal or the reciprocal of the bitrate.
- USB3.1 bitrate is 5 Gbit/s. UI (bit periods) = 1/(5 Gb/s) = 200 ps





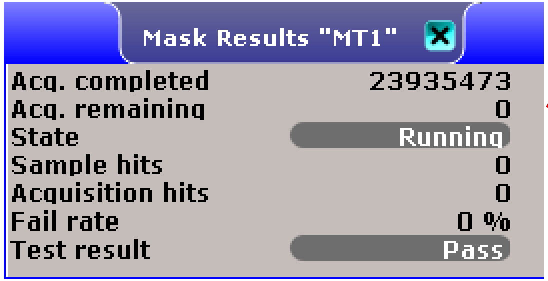
WHAT IS AN EYE DIAGRAM

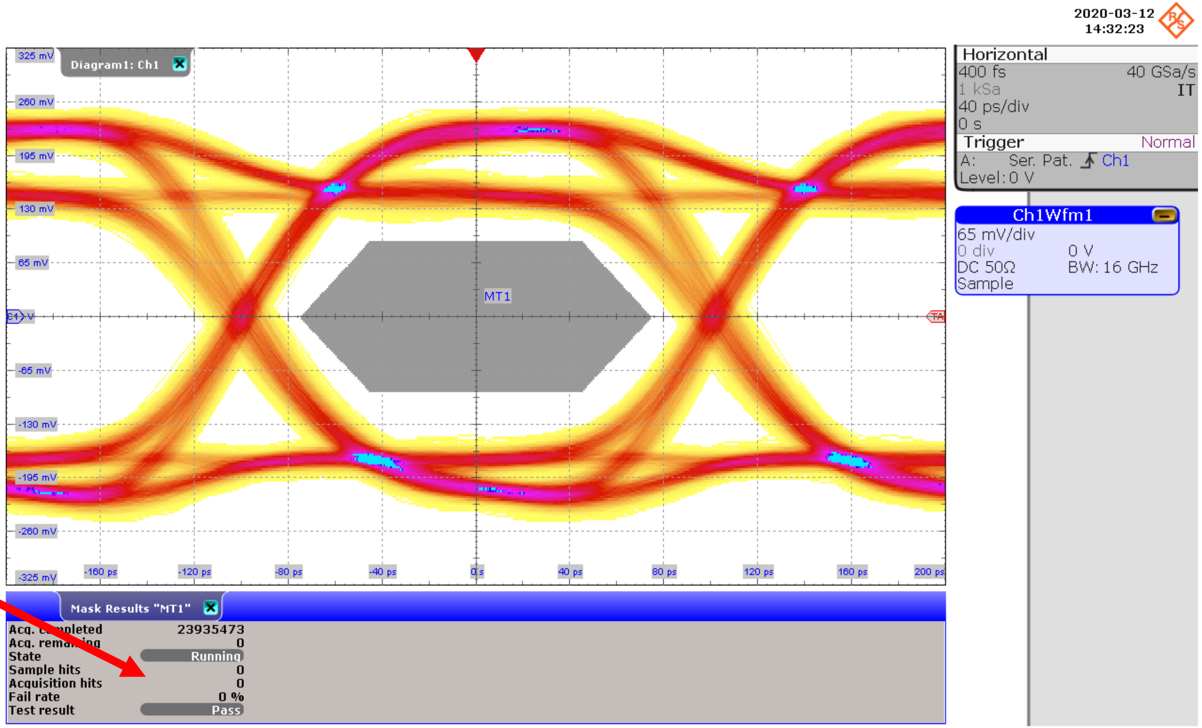
- An Eye diagram is the persistance display of all data signal’s transition (i.e 000, 111, 101, 010, 110, 001, 011);
- Eye diagram define the quality of signal.



EYE DIAGRAM MASK TEST

- Mask test can be used for compliance vs. standard.
- Statistic measurements and Pass-Fail test can be applied.



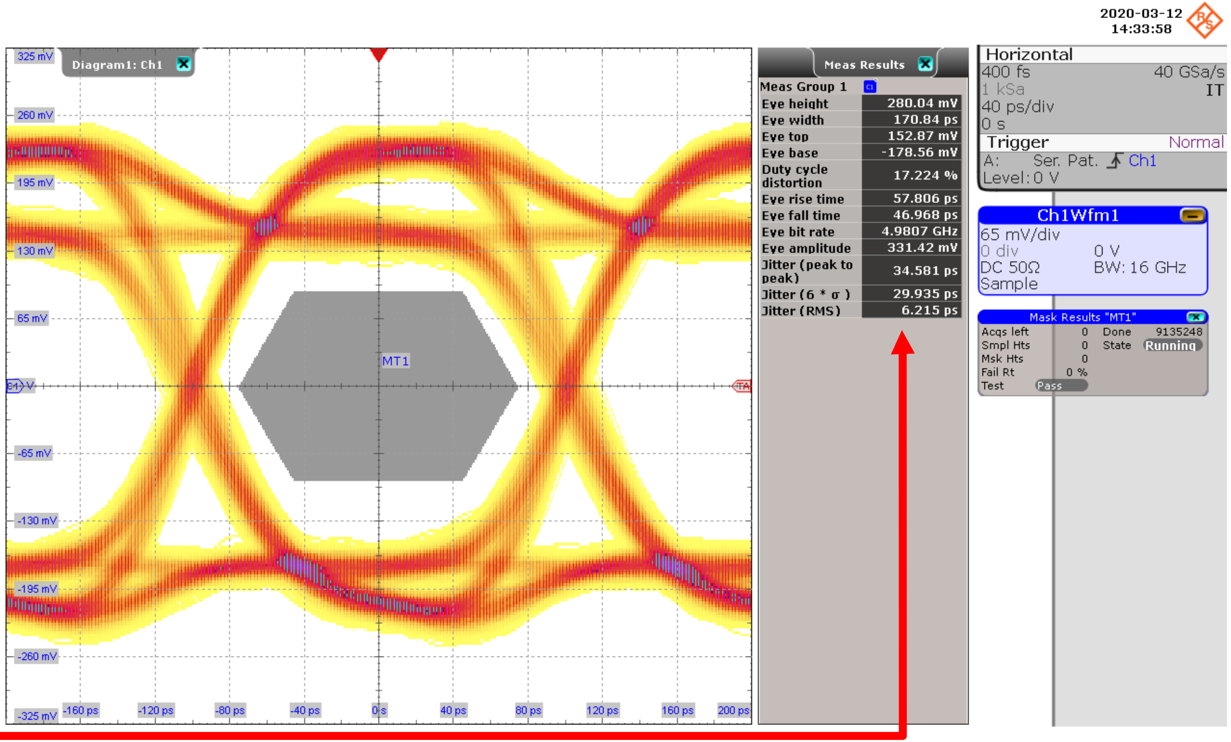


EYE DIAGRAM MEASURE

- ► Automatic Eye measuremet can be applied.

Meas Results

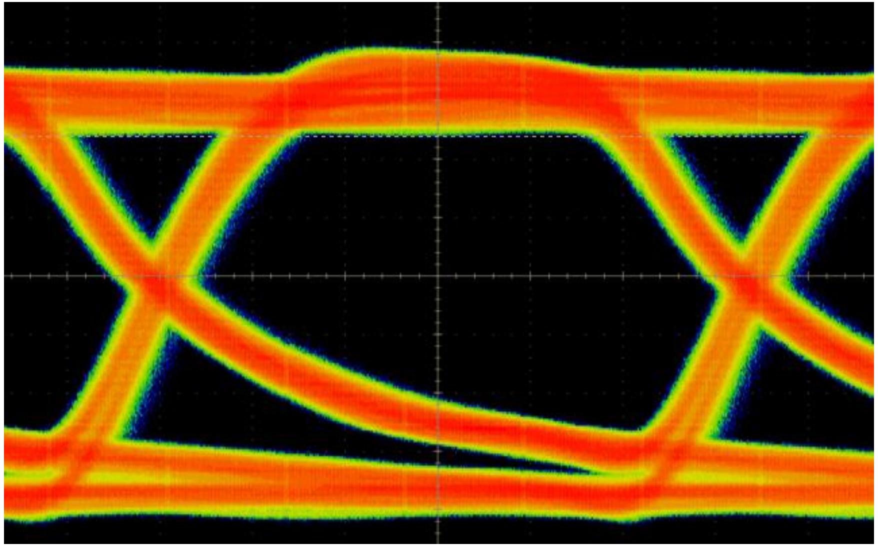
Meas Group 1	C1
Eye height	280.04 mV
Eye width	170.84 ps
Eye top	152.87 mV
Eye base	-178.56 mV
Duty cycle distortion	17.224 %
Eye rise time	57.806 ps
Eye fall time	46.968 ps
Eye bit rate	4.9807 GHz
Eye amplitude	331.42 mV
Jitter (peak to peak)	34.581 ps
Jitter (6 * σ)	29.935 ps
Jitter (RMS)	6.215 ps



METODOLOGIES FOR EYE DIAGRAM MEASUREMENTS

FAST EYE RENDERING

- Trigger oscilloscope with recovered clock
- Use display persistence to accumulate eye pattern



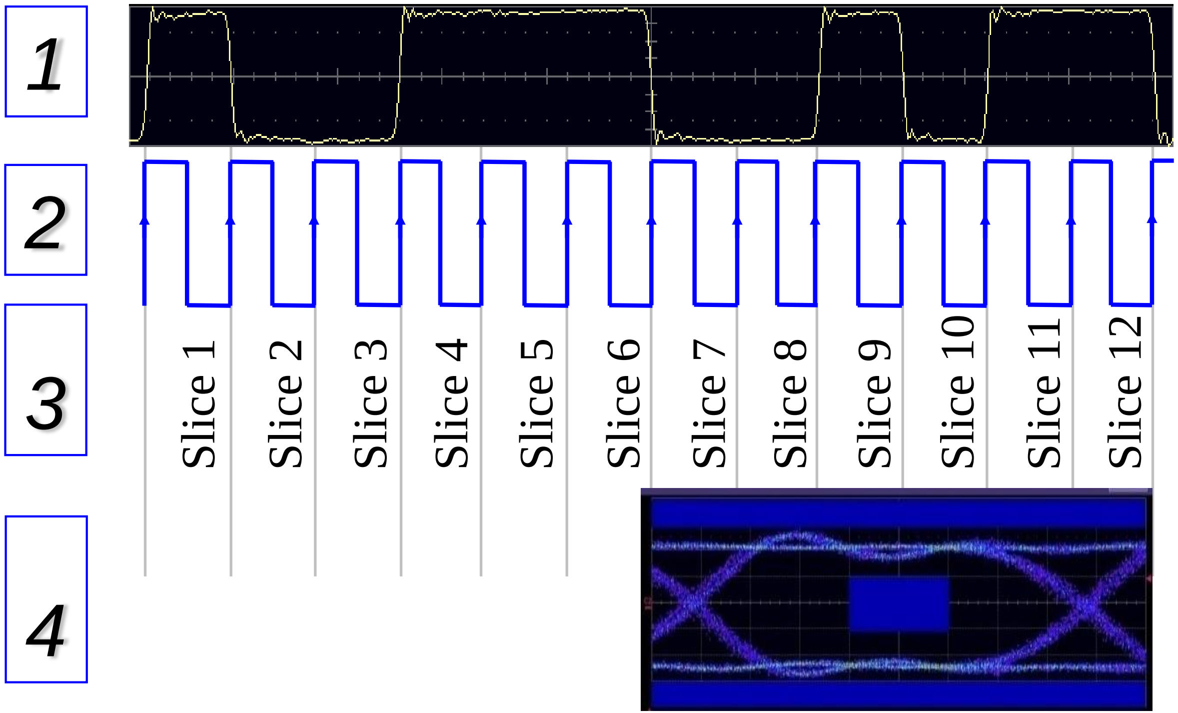
~70K acq/sec

- Pros: Unlimited data set

- Cons: Limited update rate;
- Cons: Measurement limited by trigger jitter and recovered clock jitter

«SINGLE SHOT» EYE RENDERING

► Due to high trigger jitter some oscilloscopes use a software PLL for Eye rendering :



← NRZ data record acquired from a single trigger

← Clock recovered using software "golden PLL"

← Data record divided into 1 UI segments equal to recovered clock period

← Segments overlayed to form eye pattern

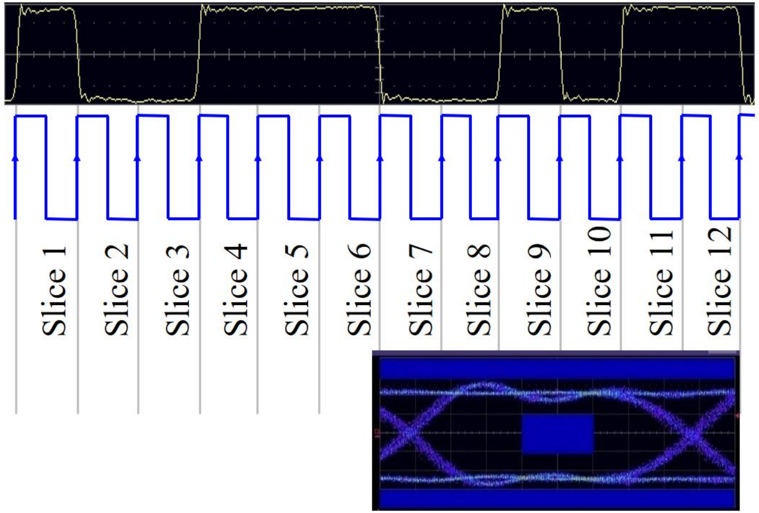
SINGLE SHOT EYE RENDERING (II)

- Pros : no trigger jitter – accurate eye diagram

- Cons: datasets (bit population) limited by acquisition memory and sample rate;

- Cons: very slow (< 10 acq/s) - sw post processing;

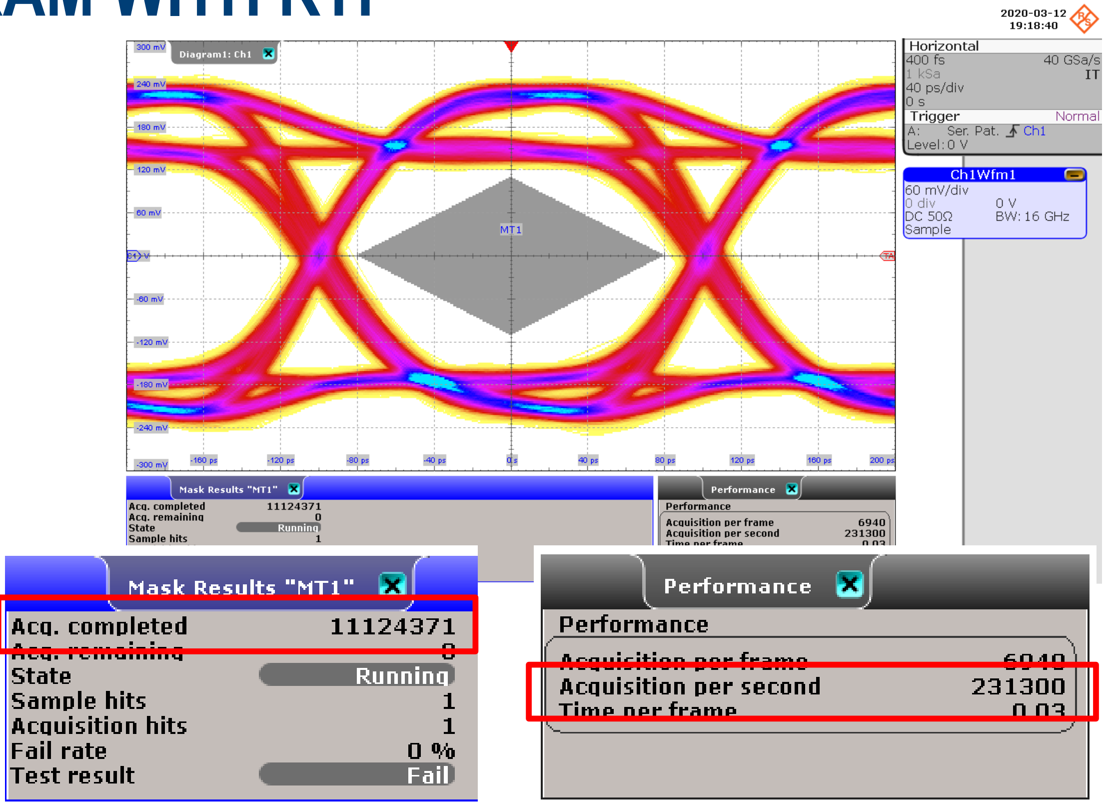
- Cons: not useful for debug – the oscilloscope stays blinded for the most of the time;



<10 acq/sec

REALT TIME EYE DIAGRAM WITH RTP

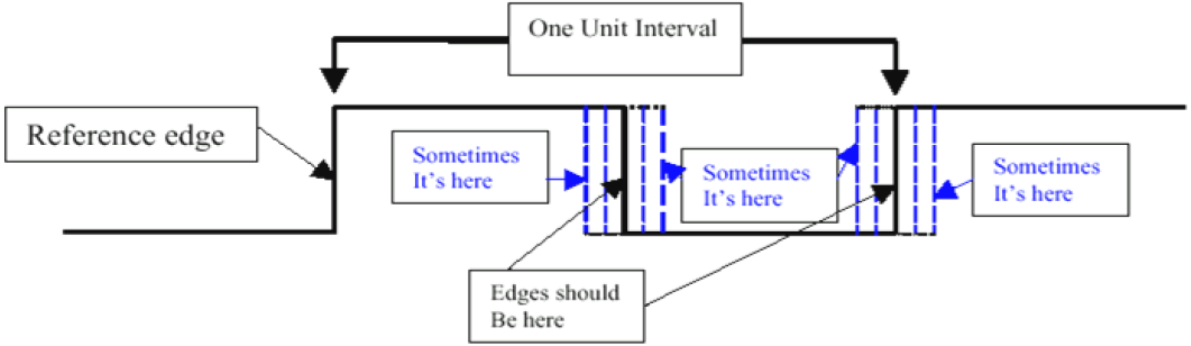
- Rely on the use of the RTP's Hw CDR up to 16 Gb/s and 160 bit pattern lenght.
- Very low intrinsic jitter due to digital trigger and CDR: similar to software implementation.
- Very fast acquisition (>200k wfms/s) and unlimited dataset – useful for debug
- Benefit from Real Time De-embedding – trigger on equalized data.



>200k acq/sec

MOTIVATION FOR JITTER DECOMPOSITION

JITTER DEFINITION



Jitter is "the short-term variations of a signal with respect to its ideal position in time"

Jitter includes instability in signal period, frequency, phase, duty cycle or some other timing characteristic.

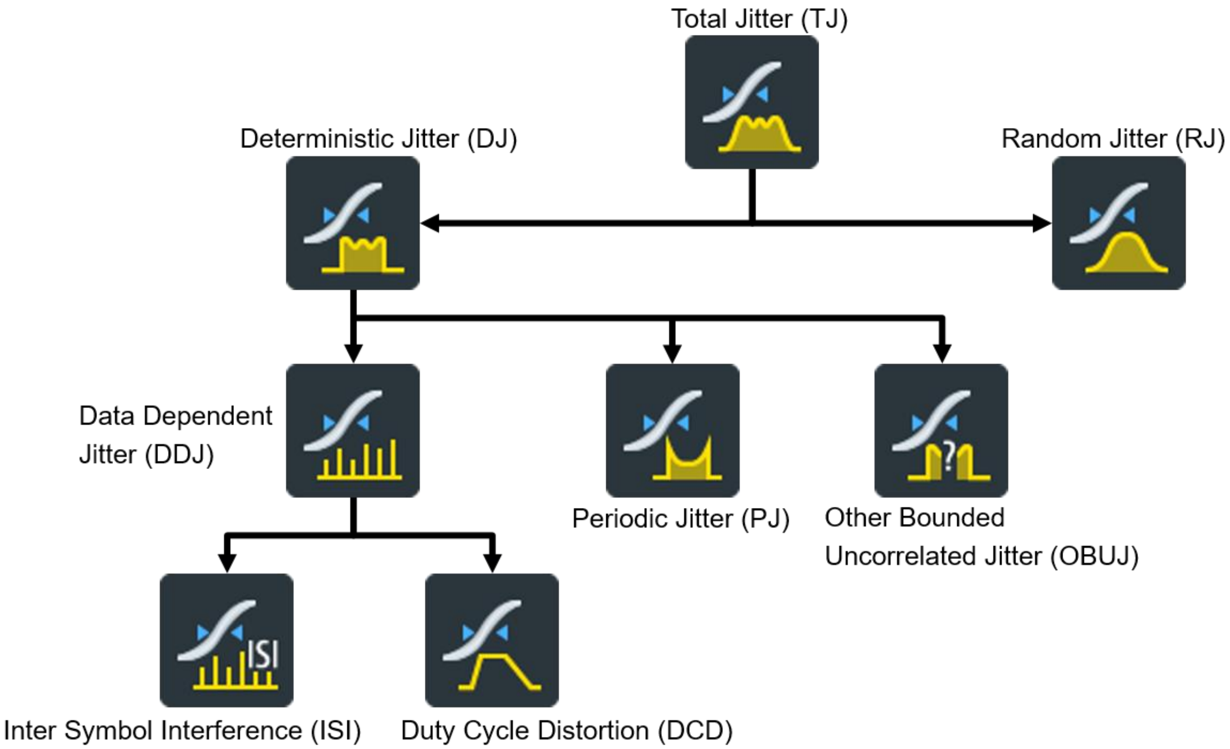
It is of interest from pulse to pulse, over many consecutive pulses, or as a longer term variation.

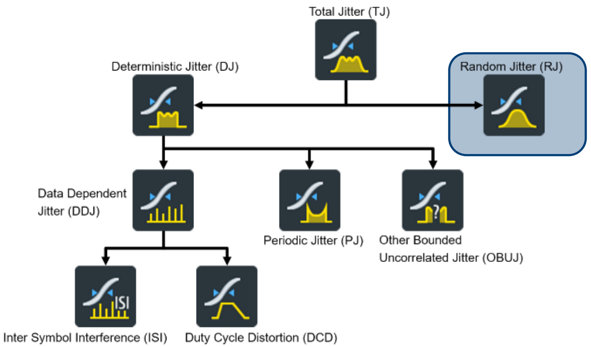
JITTER COMPONENTS

Total Jitter is composed out of several jitter contributions:

– Random Jitter: “unbounded”

– Deterministic Jitter: usually “bounded”



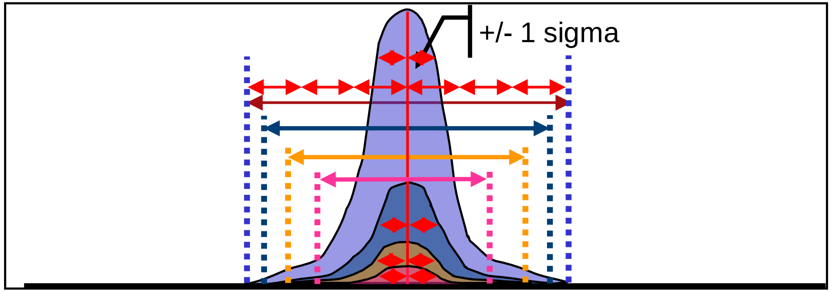


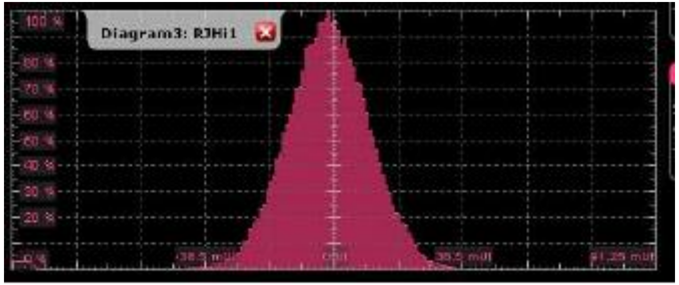
RANDOM JITTER

- Random jitter (Rj) is considered unbounded
- It can be described by a Gaussian distribution.
- It is characterized by its standard deviation (rms) value.
- The peak to peak value of random jitter will grow to without bound.

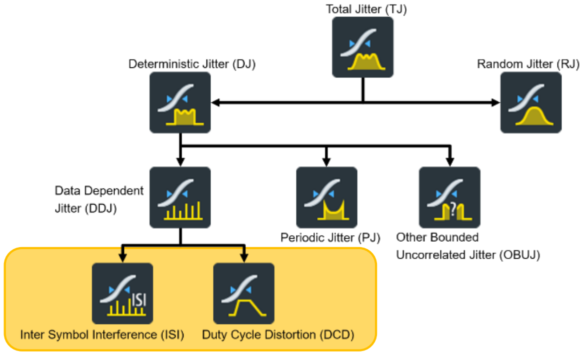
Random Jitter

- Thermal noise
- Shot noise (semiconductor dev)
- External radiation sources
- Oscillator instabilities





DETERMINISTIC JITTER

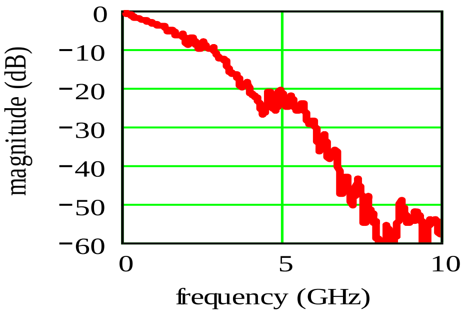


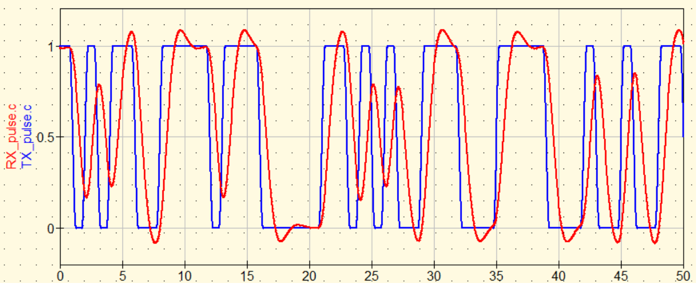
Data Dependent Jitter - ISI

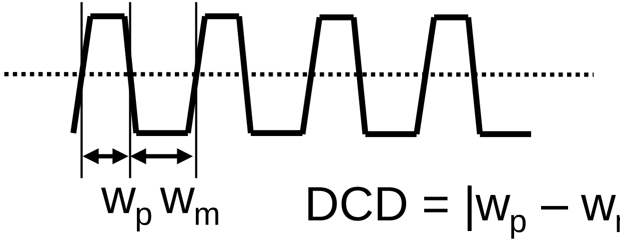
- Transmission Losses
- Circuit Bandwidth
- Frequency dependent Losses
- Dielectric Absorption
- Dispersion – esp. Optical Fiber
- Reflections, Impedance mismatch

Duty Cycle Distortion

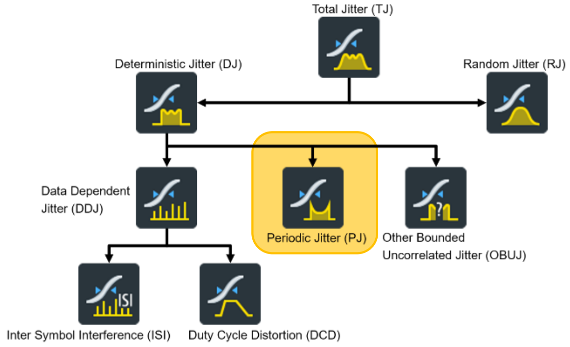
- Offset error in receiver or transmitter
- Rise/fall times mismatch







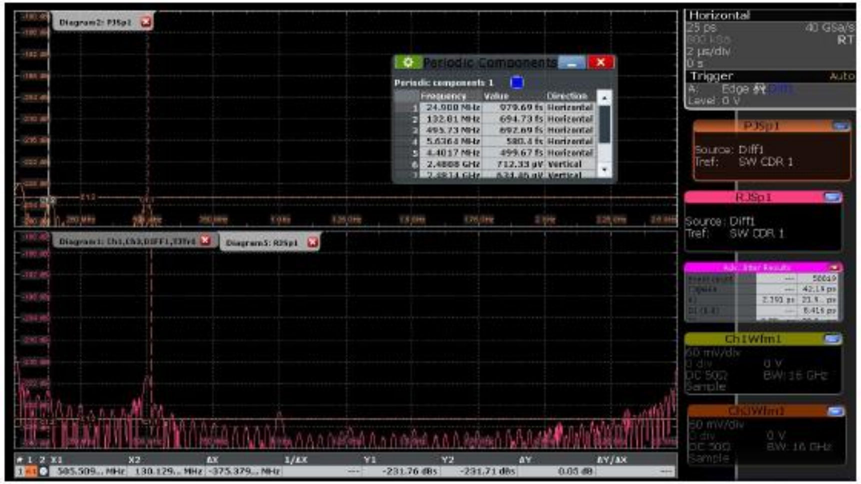
$DCD = |W_p – W_m|$



DETERMINISTIC JITTER

Periodic Jitter

- Injected noise & Circuit instabilities
- SMPS and oscillators plus harmonic content
- PLL's stability problems
- Loop bandwidth (tracking & overshoot)



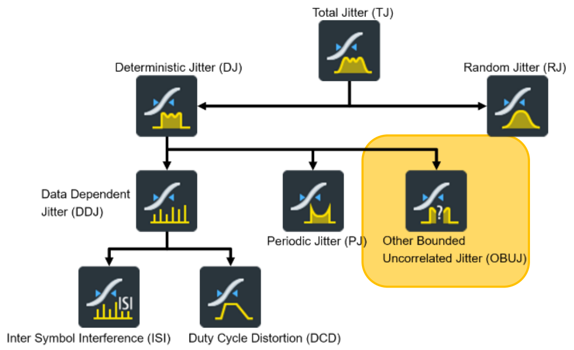
Periodic variation in the edge timing of the signal

Caused by non-data related souces

- Power supply
- Crosstalk
- EMI

Measured in the frequency domain using the jitter spectrum

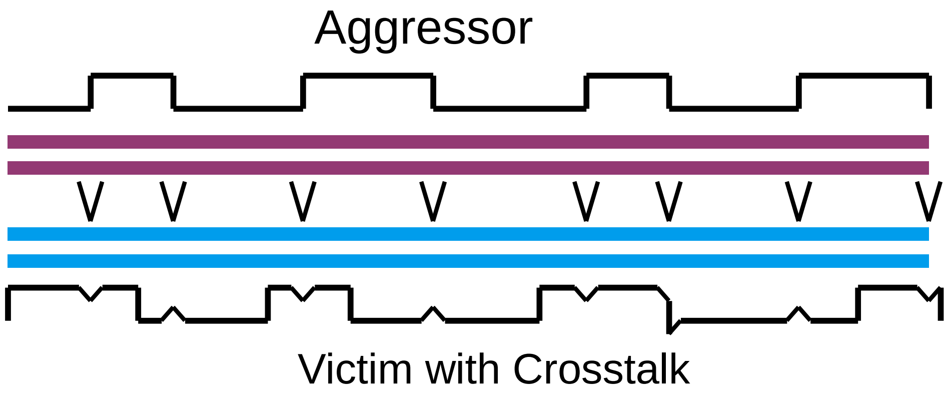
DETERMINISTIC JITTER



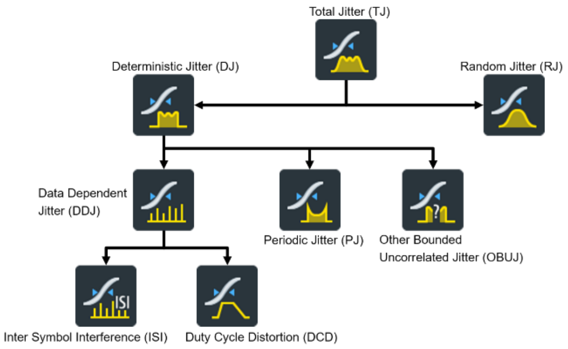
Bounded Uncorrelated Jitter (BUJ)

- X-talk from adjacent lanes (example PCIe*x)
- Appears typically as RJ without spec analysis

- Crosstalk is caused by a signal called the “aggressor” inducing a voltage or current in an adjacent conductor, the “victim”
  - Occurs during transitions where dV/dt is high
  - Fast rise time and/or high voltage swing increase crosstalk
  - Differential signaling reduces but does not eliminate crosstalk
  - Primarily affects the amplitude of the victim



HOW TO MEASURE JITTER



- Jitter can be estimated through single measurement, but…
- …. due to its nature, any measurements will show a different value.

- Random components (unbounded) will contribute differently for each new acquisition.

- RJ_{pk-pk} will grow by increasing the observation time.

- You could ask “ what is the peak-to-peak value of jitter?”
- **Question is : How long do you want to measure?**

HOW TO MEASURE JITTER (II)

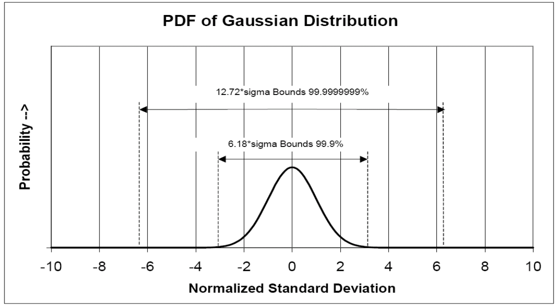
- **Industry standard define a BER value (i.e 1*10^{-12}) as reference for jitter measurement.**
- **The following equation is given by the MJSQ** (Fibrechannel Methodologies for Jitter and Signal Quality) **:**

$$\mathbf{Tj@BER = \alpha Rj_{rms} + Dj_{pk\text{-}pk}}$$

- For a given BER Rj_{rms} is normalized to a pk-pk value by **α**
- **i.e. @ BER = 10^{-12}, $\alpha \sim 14$**
- **Hence Tj= 14*Rj + Dj**

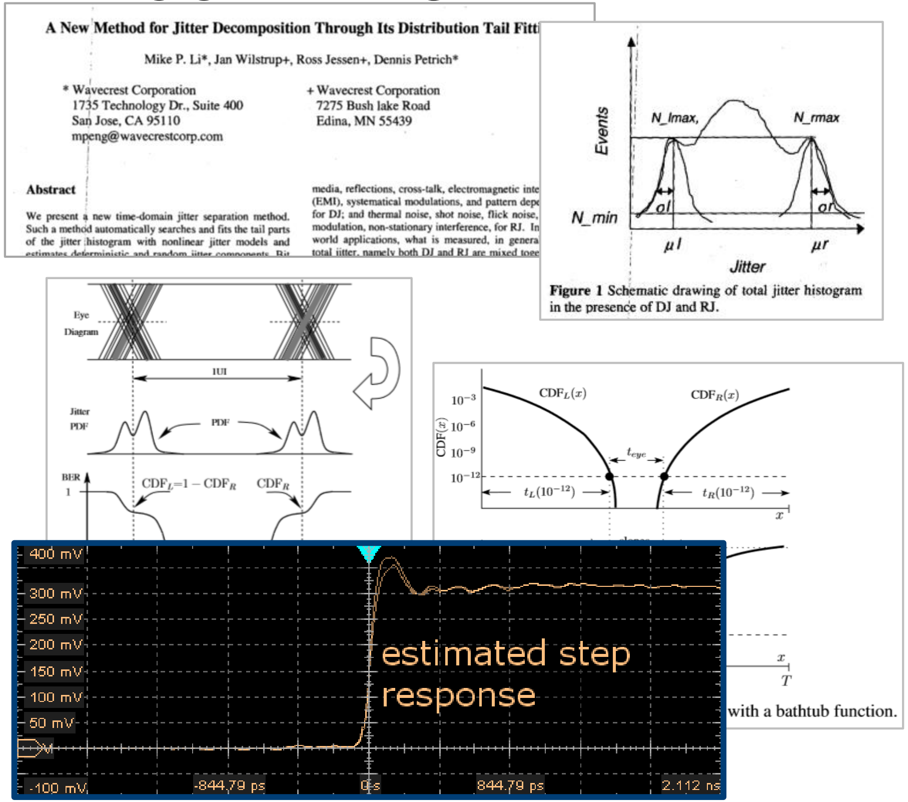
Bit Error Rate (BER)	α
10^{-9}	11.996
10^{-10}	12.723
10^{-11}	13.412
10^{-12}	14.069
10^{-13}	14.698
10^{-14}	15.301
10^{-15}	15.883
10^{-16}	16.444

Lookup table for α



TRADITIONAL SOLUTION
EVOLUTION OF DECOMPOSITION ALGORITHMS

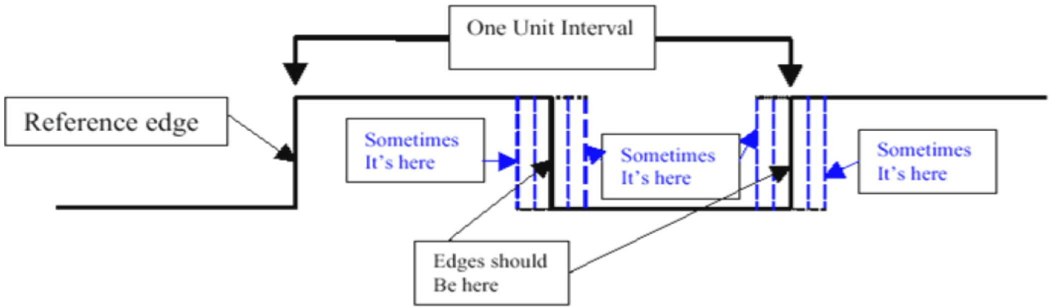
1. ~2000: Jitter Separation via „Tail“-fitting at the Histogram for RJ and DJ via Dual-Dirac-Model
2. Extension with Transformation into Q-Space
3. ~2008: Extension of Separation methods for DDJ/ISI/DDC and spectrum view for PJ, etc.
4. Extension with Noise Separation
5. **R&S novel approach: Signal-Model-based**



TIME INTERVAL ERROR (TIE)

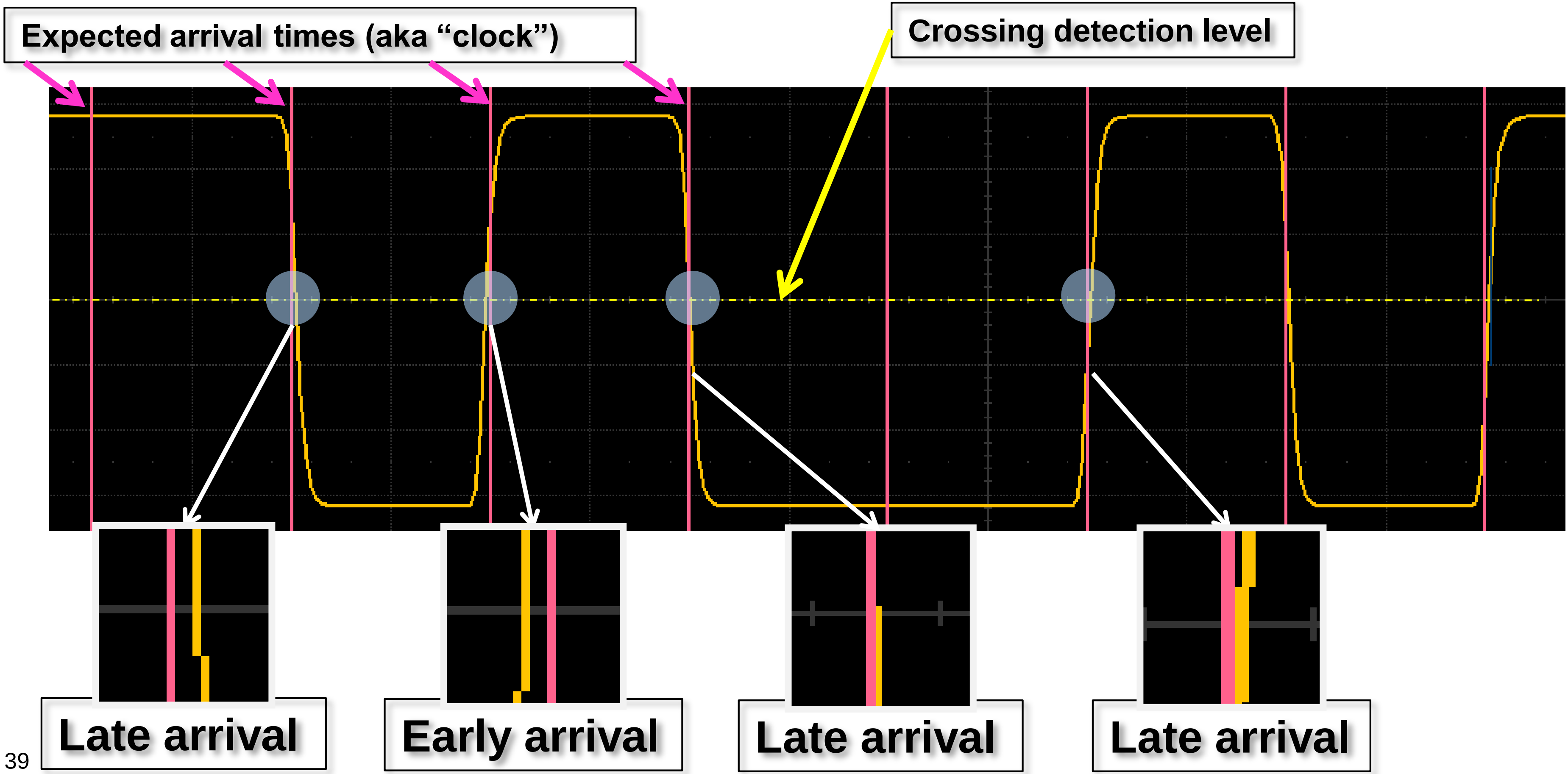
- All previous decomposition algorithms start from Time Interval Error (TIE) measure.
- TIE is the difference between the observed edge time (t_n) and the expected edge time (τ_n) for each edge present in a clock or data stream :

$$TIE_n = t_n - \tau_n$$



- Note: TIE can be applied to clock and data

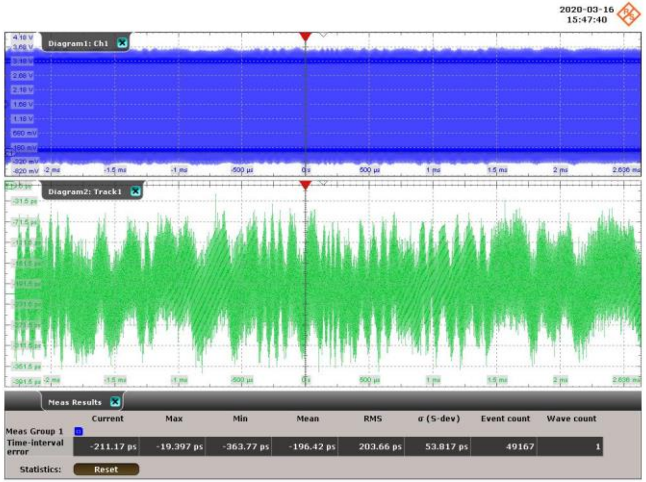
TIME INTERVAL ERROR (TIE) CONT.



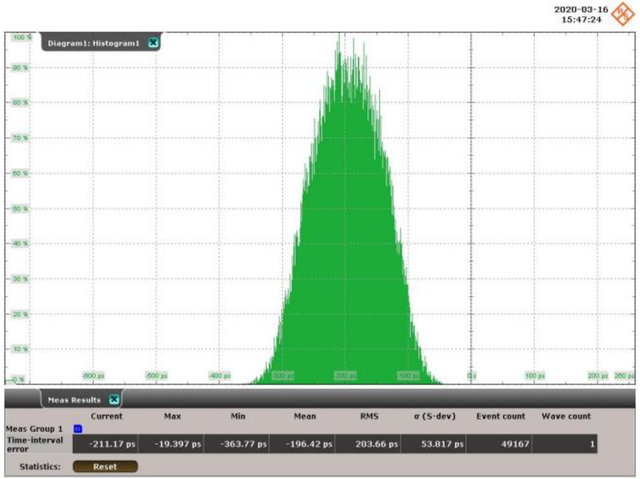
TIE MEASUREMENTS PLOT

- TIE measurements can be plotted as Track or as Histogram

TIE vs. time → TIE Track



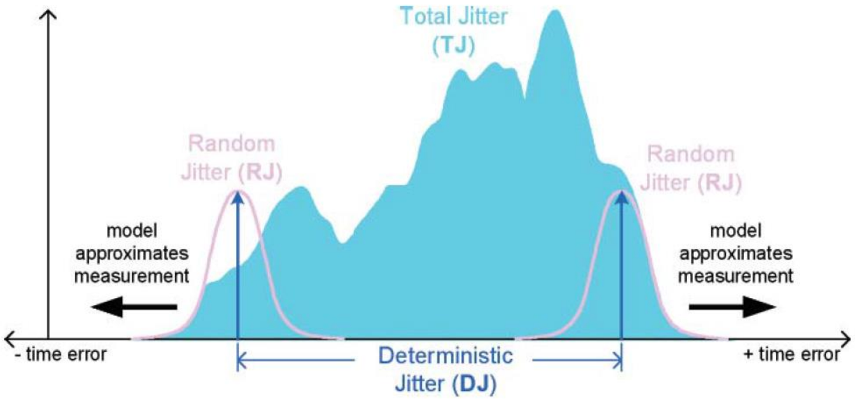
Distribution of TIE → TIE Histogram



By using sophisticated algorithm, it's possible the jitter separation from these two TIE's representation

THE DUAL DIRAC MODEL JITTER

- Fit Gaussian curves to the left and righ sides of estimates jitter PDF (i.e. the measured histogram)
- Separation of the mean values gives Dj(δ–δ)
- Standard deviation (σ) gives Rj
- Real World deterministic jitter (DJ) does not equal the dual-Dirac distribution
- Consequently Dj(δ–δ) < p2p(DJ)



$$Rj = \sigma$$

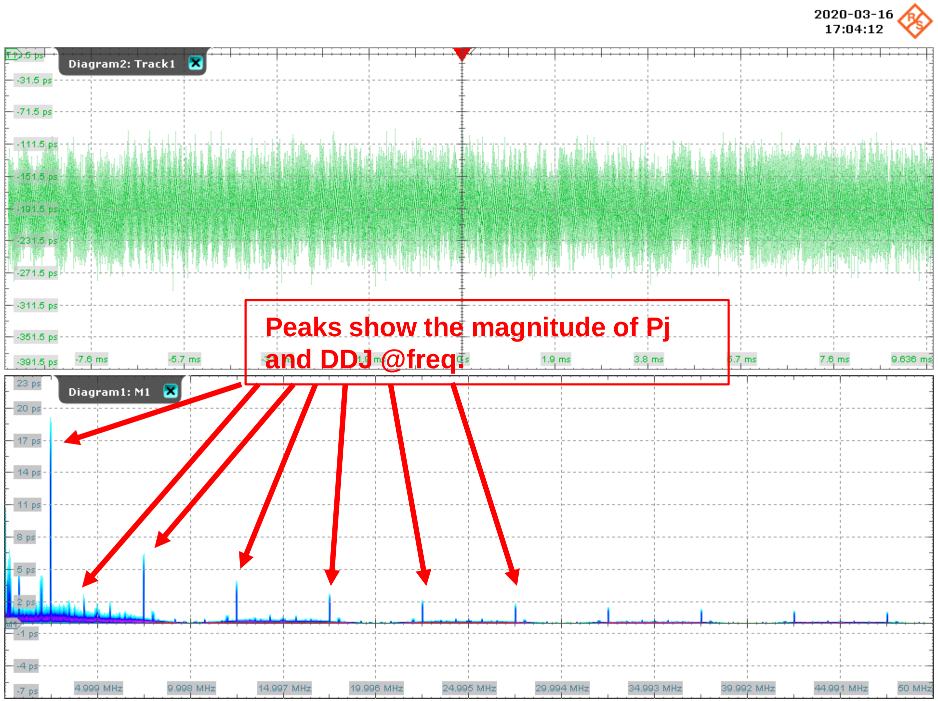
$$Dj(\delta - \delta) = \mu_R - \mu_L$$

$$Tj = Q_G(BER) * Rj + Dj(\delta - \delta)$$

SPECTRAL BASED

- **Spectrum-based methods**
  - Measure spectrum of TIE
  - Separate random from deterministic jitter by frequency content
  - Deterministic jitter is contained in the spectral "peaks"
  - Rj (σ) is measured by integrating noise floor

- The Spectral Method has 2 main assumptions
  - All of the components of Rj jitter are Gaussian
  - All components of Dj show up as peaks in the Spectrum
- Crosstalk and other types of Dj can be mistaken for Rj when they don't show up as peaks in the spectrum



THE R&S APPROACH - OVERVIEW

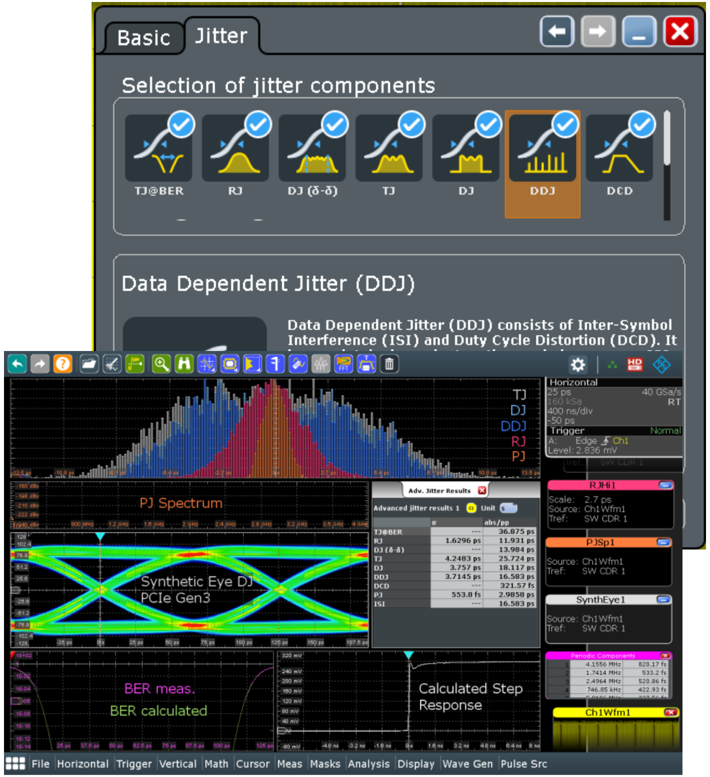
R&S ADVANCED JITTER ANALYSIS – AT A GLANCE

- New analytic approach
  - Jitter separation based on Signal Model (Step Response Estimation)
- «Signal Model» take in account the complete signal error terms, horizontal and vertical.
- All the informations of the traditional methods :
  - Break-down of Tj, Rj, Dj, DDJ, ISI, PJ
  - Histograms, Bathtub curve, etc.
- **New insight**
  - Step response display
  - Syntetic Eye for deterministic component (DDJ / DJ)
  - Pj horizontal & vertical
- *DesignCon 2020 paper**

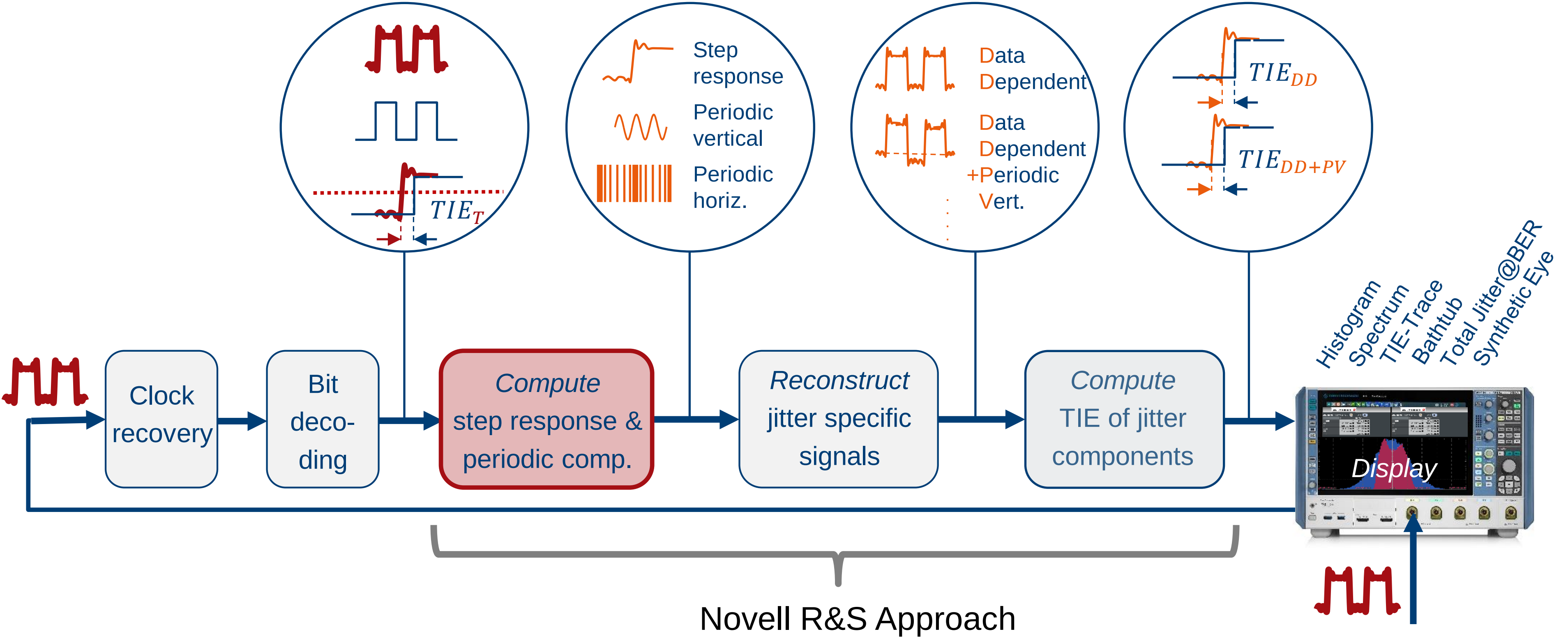
*(*available soon on R&S website)*

DesignCon 2020

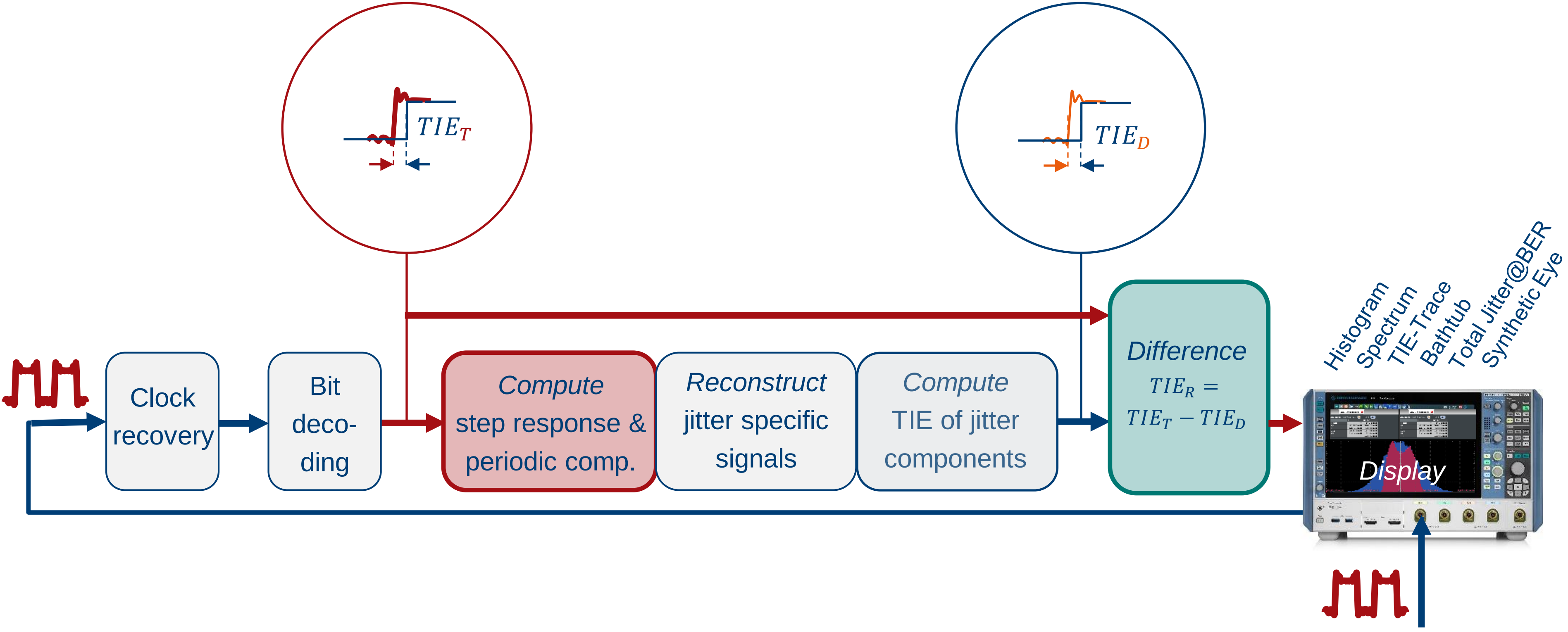
Signal Model-Based Approach to a Joint Jitter & Noise Decomposition



R&S ADVANCED JITTER DECOMPOSITION ALGORITHM DETERMINISTIC COMPONENT



R&S AVDANCED JITTER DECOMPOSITION ALGORITHM RANDOM COMPONENTS



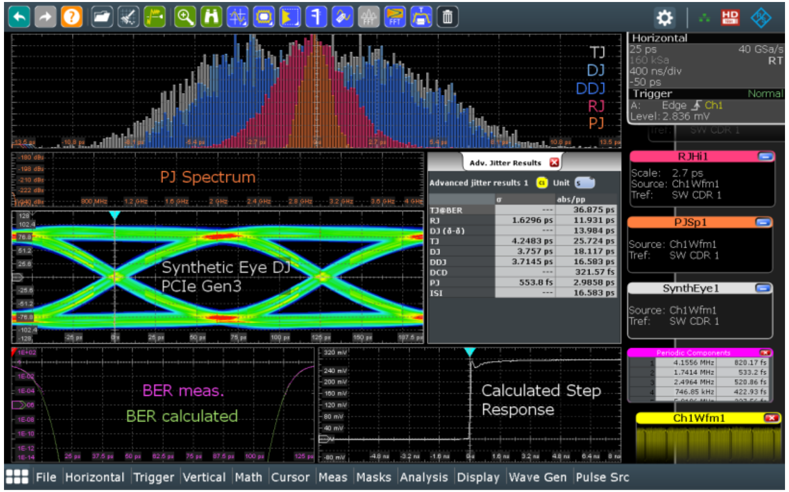
SIMPLE CONFIGURATION

1

2

3

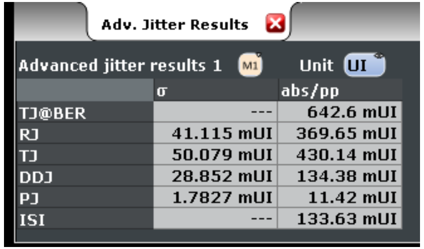
1. Configure Serial data type, PLL, etc.;
2. Select desired measurements (Tj, Rj, Dj, etc.);
3. Select what do you want to see;
4. Get results!



4

VARIOUS JITTER MEASUREMENTS AND JITTER COMPONENT SPECIFIC RESULTS

Quick 3 step setup & explanation of each Jitter componenet


Adv. Jitter Results

Advanced jitter results 1 — Unit UI

	σ	abs/pp
TJ@BER	---	642.6 mUI
RJ	41.115 mUI	369.65 mUI
TJ	50.079 mUI	430.14 mUI
DDJ	28.852 mUI	134.38 mUI
PJ	1.7827 mUI	11.42 mUI
ISI	---	133.63 mUI

Various jitter results:

- Standard deviation and peak-peak values
- Total Jitter@BER
- Duty Cycle Distortion (DCD)
- Inter Symbol Interference (ISI)
- DJ dual dirac

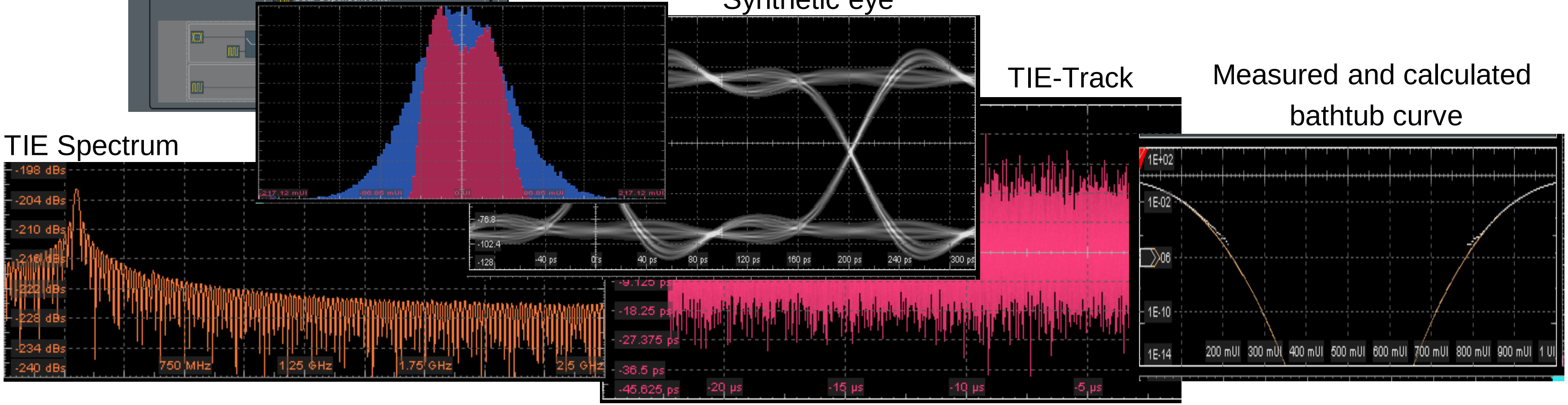
Histograms

Synthetic eye

TIE-Track

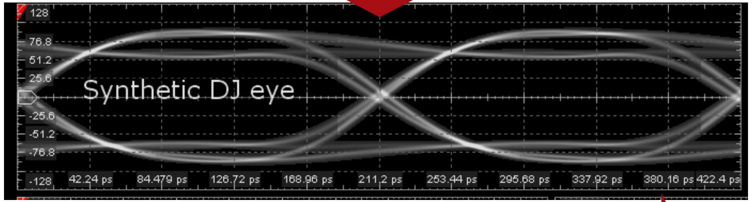
Measured and calculated bathtub curve

TIE Spectrum



NEW INSIGHTS

Synthetic eye

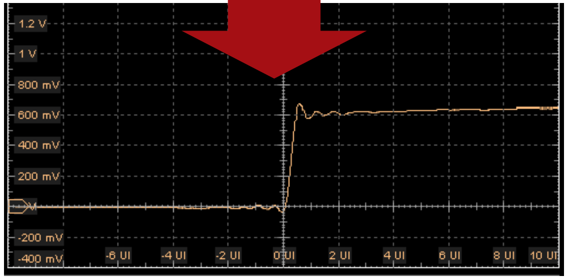


Periodic Components

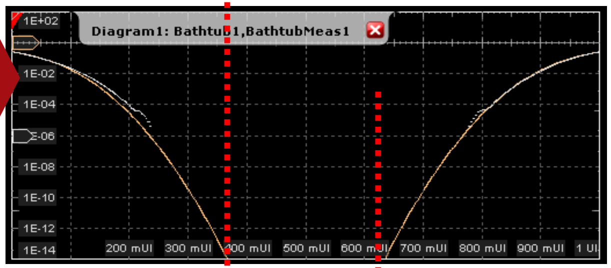
Periodic components 1

	Frequency	Value	Direction
1	35.502 MHz	12.947 ps	Horizontal
2	58.19 MHz	365.11 fs	Horizontal
3	5 GHz	7.1649 mV	Vertical
4	7.1608 GHz	354.19 µV	Vertical
5	4.1 GHz	320.02 µV	Vertical

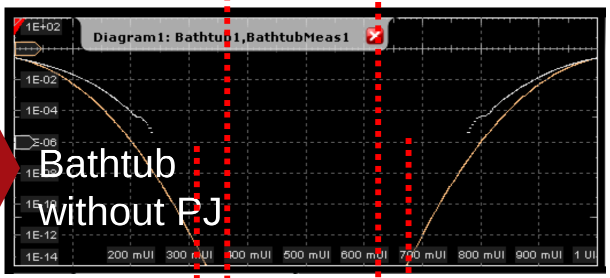
Step response



Bathtub
Total Jitter

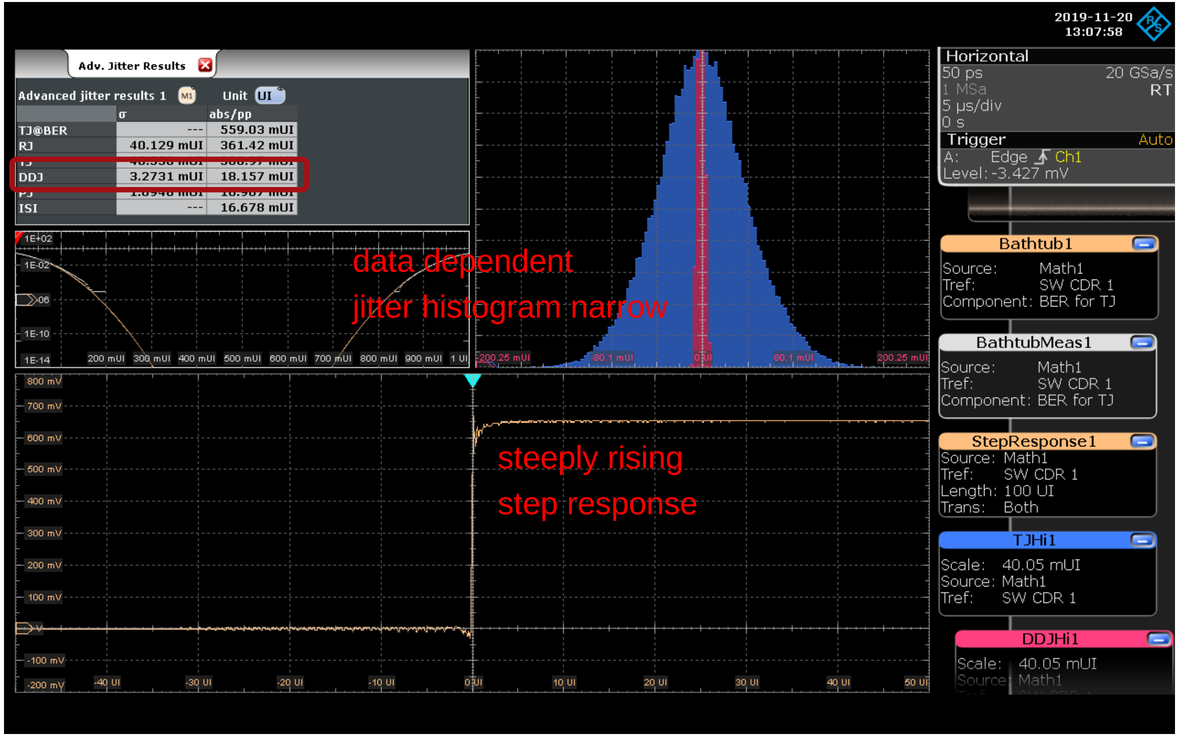


What-if Bathtub
DDJ+RJ only
assuming no
periodic jitter



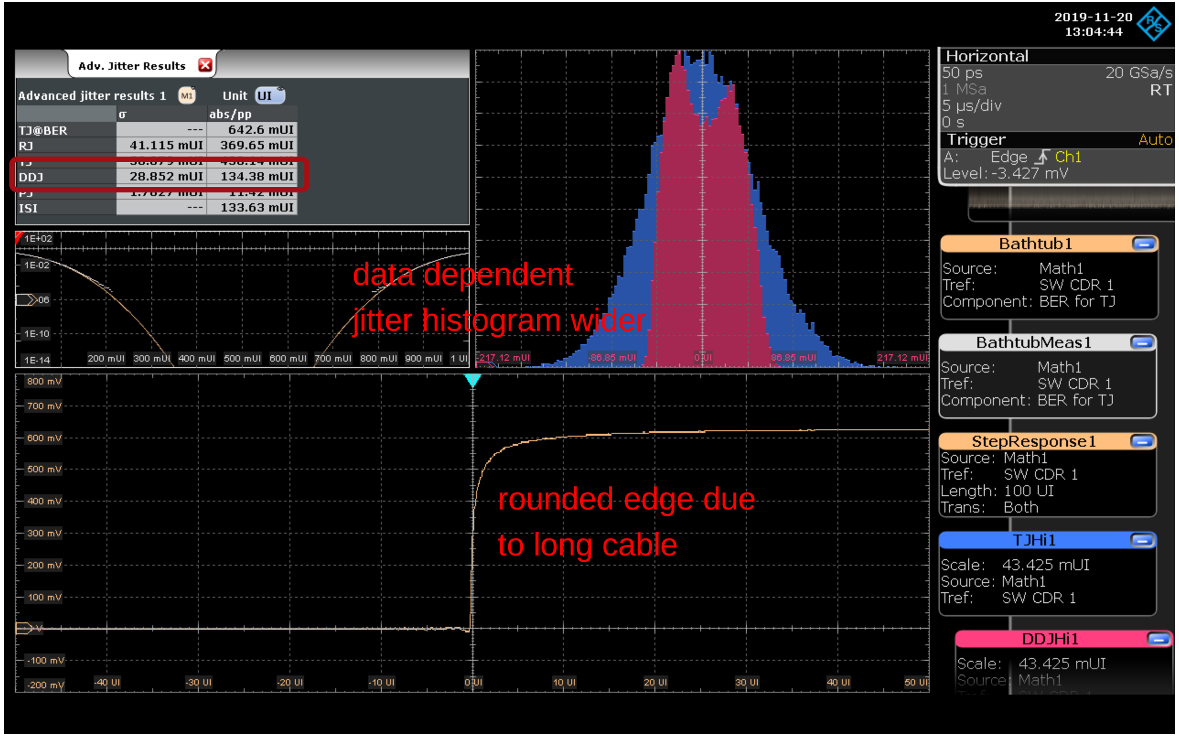
EXAMPLE - 35 CM CABLE

- Short cable causes minimal deviation from ideal step
- Relatively low Data Dependent Jitter (DDJ): 18 mUI peak-peak
- DDJ histogram narrow as expected
- Rj(rms) ~ 40 mUI



EXAMPLE - 2 M CABLE

- Long cable causes significant deviation from ideal step
- Large Data Dependent Jitter (DDJ): 134 mUI peak-peak
- DDJ histogram wide. (significant jitter component)
- Rj(rms) ~ 41 mUI, consisten with previous measurement.

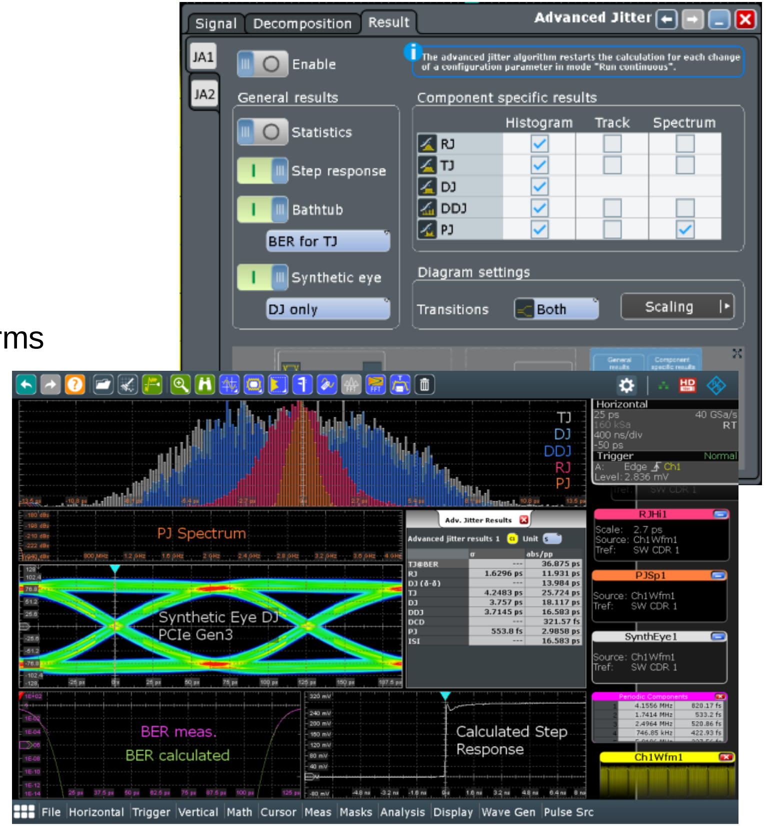


EYE AND JITTER LIVE DEMO

BASIG OF SIGNAL INTEGRITY – PART I
SUMMARY

- What is an eye diagarm and what information we can get;
- Why measure jitter and why separation is important
- R&S decomposition algorithm :
  - uses all signal information
  - Based on Signal model instead of TIE model
  - Uses all signal information, incluse horizontal and vertical error terms
  - More results details available
  - Consistent results for Decomposition and BER estimation

- More results for in-depth analysis
  - Step Response display
  - Synthetic eye for deterministic components
  - Periodic jitter: vertical and horizontal components, etc.



MORE INFORMATION

► RTP web page :

https://www.rohde-schwarz.com/it/prodotto/rtp-pagina-iniziale-del-prodotto_63493-469056.html

► Adv. Jitter

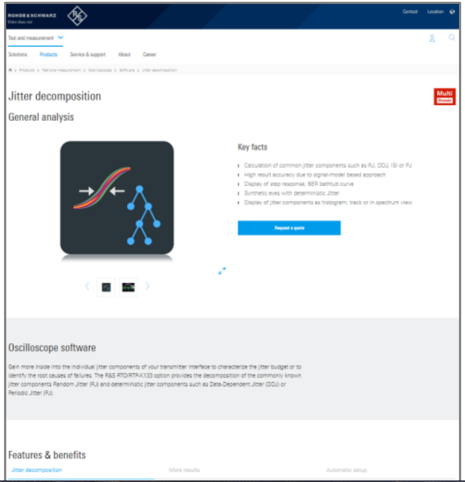
– Application web page

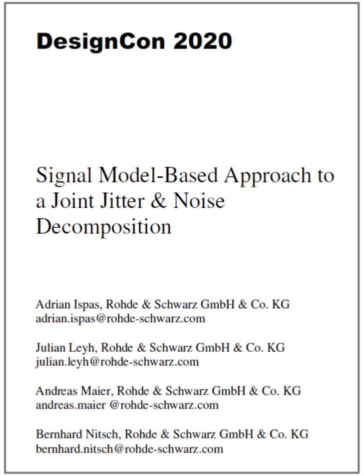
https://www.rohde-schwarz.com/product/sw_rtx-k133-productstartpage_63493-732992.html

Application Video web page

https://www.rohde-schwarz.com/products/test-and-measurement/oscilloscopes/rtp-videos/rtp-video-list_250788.html?change_c=true

DesignCon paper

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Signal Model-Based Approach to a Joint Jitter & Noise Decomposition

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Application Video